

This listing of claims will replace all prior versions, and listings, of claims in the application:

**The Status of the Claims**

1. (Cancelled)
2. (Cancelled)
3. (Cancelled)
4. (Cancelled)
5. (Cancelled)
6. (Cancelled)
7. (Cancelled)
8. (Cancelled)
9. (Cancelled)

10. (Cancelled)

11. (Cancelled)

12. (Original) A metal line structure formed in a semiconductor device, comprising:

first metal lines formed on a substrate, the first metal lines having a first barrier metal layer and a first conductive layer;

a first interlayer insulator between adjacent ones of the first metal lines;

second metal lines formed on respective ones of the first metal lines, the second metal lines having a second barrier metal layer and a second conductive layer; and

a second interlayer insulator between adjacent ones of the second metal lines.

13. (Original) A metal line structure as defined in claim 12, wherein each of the first metal lines has about 50% of a desired thickness of the metal line structure.

14. (Original) A metal line structure as defined in claim 12, wherein the first metal lines comprises an Al alloy containing 5% or less.

15. (Original) A metal line structure as defined in claim 12, wherein the second interlayer insulator has about 50% of a desired thickness

of the desired metal line structure.

16. (Original) A metal line structure as defined in claim 12, wherein the second conductive layer comprises Cu.

17. (Original) A metal line structure as defined in claim 12, wherein the first interlayer insulator is made of USG or FSG deposited by an HDP process.

18. (Original) A metal line structure as defined in claim 12, wherein the second interlayer insulator is made of USG or FSG deposited by a PECVD process.

19. (Original) A metal line structure as defined in claim 12, wherein the second interlayer insulator is made of USG or FSG deposited by a PECVD SiOC.

20. (Original) A metal line structure as defined in claim 12, wherein the first and the second barrier metal layers comprise at least one of Ti, TiN, Ta, TaN, W and WN.